Recent Research on Memristor Based Circuits

Herbert H.C. Iu

School of Electrical, Electronic and Computer Engineering
The University of Western Australia, Australia

Presented by H. Iu
December 2016
Contents

- Research team
- Introduction of memristor
- Memristor based chaotic circuit
- Universal mutator for transformations among memristor, memcapacitor and meminductor
- Coupled memristors
- Future work
Research team

**Power and Clean Energy (PACE) Research Group**

- Group Leaders – Prof Tyrone Fernando and Prof Herbert Iu
- 10 PhD students
  - Power Electronics, Nonlinear Systems, Smart Grid, Renewable Energy Systems etc...
- 1 Emeritus Professor
Research areas

- Switching dc/dc converters
- Power factor correction circuits
- Renewable energy
- Smart grid
- Memristor based circuits
Memristor

- **What is a memristor?**
- It is the missing 4\textsuperscript{th} element postulated by L.O. Chua in 1971 [1].
- Researchers in Hewlett-Packard announced a solid state implementation of memristors in 2008 [2].

The four elements in circuit theory

- \( q = \int i \, dt \), where \( q \) is the charge
- \( \varphi = \int v \, dt \), where \( \varphi \) is the flux
Circuit theory of memristor

1. Charge-controlled memristor
   - $v = M(q) \ i$, where $M(q) = d\phi/dq$. $M$ is called memristance.

2. Flux-controlled memristor
   - $i = W(\phi) \ v$, where $W(\phi) = dq/d\phi$. $W$ is called memductance.
How memristance works?

How memristance works?

HP memristor

- HP memristor is in the form of a partially doped TiO$_2$ thin film with platinum electrodes.

- \[ M(w) = R_{ON} \left( \frac{w(t)}{D} \right) + R_{OFF} \left( 1 - \frac{w(t)}{D} \right), \]

- \[ w(t) = \mu_v \left( \frac{R_{ON}}{D} \right) q(t), \]

where \( D \) is the total width of TiO$_2$ film, \( w(t) \) is the width of the region of high dopant concentration on the film, \( R_{OFF} \) and \( R_{ON} \) are the limit values of the memristance for \( w(t) = 0 \) and \( w(t) = D \), \( \mu_v \) is the dopant mobility.
Fingerprint - Pinched hysteresis loop

![Graph showing pinched hysteresis loop](image)
Classification


1. Ideal memristor

2. Generic memristor

3. Extended memristor
Ideal memristor

**Current-controlled**

- $v = M(q) i; \quad dq/dt = i.$

**Voltage-controlled**

- $i = W(\varphi) v; \quad d\varphi/dt = v.$
Generic memristor

Current-controlled

\[ v = M(x) \, i; \quad \frac{dx}{dt} = f(x, i). \]

Voltage-controlled

\[ i = W(x) \, v; \quad \frac{dx}{dt} = g(x, v). \]
Extended memristor

**Current-controlled**

\[ v = M(x, i) \; i \; ; \; M(x,0) \neq \infty \; ; \; \frac{dx}{dt} = f(x,i). \]

**Voltage-controlled**

\[ i = W(x, v) \; v \; ; \; W(x,0) \neq \infty \; ; \; \frac{dx}{dt} = g(x,v). \]
Motivation

- Memristor will have a lot of potential applications, and some of them will be related to nonlinear dynamics.

- The characteristics and dynamical behaviour of memristor based systems should be studied in detail.

- Recent studies show that memristor can play a major role in nonlinear systems.
Memristor based chaotic circuit


- $\phi(t)$ denotes the magnetic flux between two terminals of a memristor, assume $q = a\phi + b\phi^3$
- $W(\phi(t))$ is the memductance function, $W(\phi(t)) = a + 3b\phi(t)^2$
# Simulation parameters

<table>
<thead>
<tr>
<th>Simulation parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance $L$</td>
<td>10.8mH</td>
</tr>
<tr>
<td>Capacitance $C_1, C_2$</td>
<td>6.8nF, 268nF</td>
</tr>
<tr>
<td>Resistance $R$</td>
<td>1800Ω</td>
</tr>
<tr>
<td>Time constant $\tau$</td>
<td>1220</td>
</tr>
<tr>
<td>$a$</td>
<td>0.0007</td>
</tr>
<tr>
<td>$b$</td>
<td>0.00004</td>
</tr>
</tbody>
</table>
Phase portraits

- Chaotic state
  \[ R = 1800\Omega \]

- Periodic state
  \[ R = 1600\Omega \]
Power spectrum diagrams

- Chaotic state
- Periodic state
Bifurcation diagrams

- \( \Phi \) vs \( R \)

- \( v_1 \) vs \( R \)
Twin-T notch filter

\[
\begin{align*}
&\frac{dv_{n1}(t)}{dt} = q \frac{dv_{in}(t)}{dt} + \frac{0.5v_{in}(t) + (2q^2 - 2q + 0.5)v_{o}(t) + (2q - 1)v_{n1}(t) - 2qv_{n2}(t)}{R_n C_n} \\
&\frac{dv_{n2}(t)}{dt} = \frac{dv_{in}(t)}{dt} - \frac{2v_{n2}(t) - (2q - 1)v_{o}(t) - v_{n1}(t)}{R_n C_n} \\
&\frac{dv_{o}(t)}{dt} = \frac{dv_{in}(t)}{dt} - \frac{2v_{n2}(t) - 2(q - 1)v_{o}(t) - 2v_{n1}(t)}{R_n C_n}
\end{align*}
\]
Input-output transfer function

\[ F(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{s^2 + \frac{1}{R_n^2 C_n^2}}{s^2 + \frac{4}{R_n C_n} (1 - q)s + \frac{1}{R_n^2 C_n^2}} \]
Schematic of the MCC with notch filter controller
Experimental prototype
Results of notch filter control
Experimental results - phase portraits

- $v_2$ vs $\phi$
- $V_2$ vs $V_1$
Experimental results - power spectrum

- Before connection - Chaotic state
- After connection - Periodic state
Memristor emulator


- Emulator consists of 4 current conveyors, 1 op amp, 1 multiplier, 1 capacitor and several resistors.

\[ i_{\text{MR}} = v_{\text{AB}} \cdot \frac{R_4(R_8 + R_9)}{10R_3R_8R_{10}} \left( \frac{R_7}{R_5} \frac{1}{R_3C_1} \varphi_{\text{AB}} - \frac{R_7}{R_6}v_s \right) \]

- \( W(\varphi(t)) \) is the memductance.

\[ W(\varphi_{\text{AB}}) = \alpha \varphi_{\text{AB}} + \beta \]

\[ \alpha = \frac{R_4R_7(R_8 + R_9)}{10R_3^2R_5C_1R_8R_{10}}, \quad \beta = -\frac{R_4R_7(R_8 + R_9)}{10R_3R_6R_8R_{10}}v_s \]
Serial and Parallel Connections

- **Graphs:**
  - **Left Graph:** Plots $i_{MR}$ (mA) against $V_{AB}$ (V) showing both serial and parallel connections.
  - **Right Graph:** Plots Memductance (mS) against time (s) with separate curves for parallel and serial connections.

- **Icons:**
  - **Serial Icon:** Represented by a line with a dot in the middle.
  - **Parallel Icon:** Represented by a line with a cross.

- **Equations:**
  - $i_{MR}$ (mA)
  - Memductance (mS)
  - $V_{AB}$ (V)
  - $t$ (s)

- **Additional Notes:**
  - The graphs illustrate the behavior of current and memductance in both serial and parallel connections.
Introduction of Memcapacitor


Voltage-controlled

\[ q = C \left( \int_{t_0}^{t} V_C(\tau) d\tau \right) \cdot V_C \]

Charge-controlled

\[ V_C = C^{-1} \left( \int_{t_0}^{t} q(\tau) d\tau \right) \cdot q \]
Introduction of Meminductor

Current-controlled

\[ \varphi = L \left( \int_{t_0}^{t} I(\tau) d\tau \right) \cdot I \]

Flux-controlled

\[ I = L^{-1} \left( \int_{t_0}^{t} \varphi(\tau) d\tau \right) \cdot \varphi \]
A Universal Mutator


- Mutator consists of 3 common transimpedance operational amplifiers (TOAs)
- Position 4 is used for memory elements.
- Positions 1, 2, 3 and 5 contain only resistors or capacitors.
Case study: MR to MC

- At position 4,
  \[ G_m = \alpha \varphi_{\text{MR}} + \beta \]

- From terminal AB,
  \[ C_m = G_m C_1 R_3 R_5 / R_2 \]
MR to MC : Experimental Results

Measured pinched hysteretic loops

Variation curve of $C_m$ along with terminal voltages

$C_m = 1.64\mu F$

$C_m = 3.95\mu F$
Summary of Transformations

Table 1 Combination case 1 and corresponding transformed memconductance

<table>
<thead>
<tr>
<th>Transformation</th>
<th>Connection combinations</th>
<th>Memconductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR→MC</td>
<td>$C_1 \ R_2 \ R_3 \ G_m \ R_5$</td>
<td>$C_m = \frac{G_m C_1 R_2 R_5}{R_2}$</td>
</tr>
<tr>
<td>MC→MR</td>
<td>$R_1 \ R_2 \ R_3 \ C_m \ C_5$</td>
<td>$G_m = \frac{C_m R_3}{R_1 R_2 C_5}$</td>
</tr>
<tr>
<td>MC→MI</td>
<td>$R_1 \ R_2 \ C_3 \ C_m \ C_5$</td>
<td>$F_m = \frac{C_m R_3}{R_1 R_2 C_3 C_5}$</td>
</tr>
<tr>
<td>MI→MC</td>
<td>$C_1 \ C_2 \ R_3 \ F_m \ R_5$</td>
<td>$C_m = \frac{F_m C_1 C_2 R_3 R_5}{R_5}$</td>
</tr>
<tr>
<td>MR→MI</td>
<td>$R_1 \ R_2 \ C_3 \ G_m \ R_5$</td>
<td>$F_m = \frac{G_m R_5}{R_1 R_2 C_3}$</td>
</tr>
<tr>
<td>MI→MR</td>
<td>$R_1 \ C_2 \ R_3 \ F_m \ R_5$</td>
<td>$G_m = \frac{F_m C_2 R_3 R_5}{R_1}$</td>
</tr>
</tbody>
</table>
Coupled Memristors


Flux controlled memristor model:

\[ i(t) = W(\varphi)v(t) \]

\[ W(\varphi) = \frac{dq(\varphi)}{d\varphi} \]

\[ W(\varphi) = \alpha\varphi + \beta \]

A flux controlled and coupled ideal MR system:

\[ i_1(t) = W_1(\varphi_1, \varphi_2)v_1(t) \]

\[ i_2(t) = W_2(\varphi_1, \varphi_2)v_2(t) \]

\[ \frac{d\varphi_1}{dt} = v_1(t) \]

\[ \frac{d\varphi_2}{dt} = v_2(t) \]
A Flux Controlled and Coupled Ideal MR system

\[ W_1(\varphi_1, \varphi_2) = \alpha_1 \varphi_1 + \beta_1 + \kappa_2 \varphi_2 \]

\[ W_2(\varphi_2, \varphi_1) = \alpha_2 \varphi_2 + \beta_2 + \kappa_1 \varphi_1 \]
Coupled MRs in Serial Connections

Serial MR Circuit with Identical Polarities

\[ v_{12} = v_1 + v_2 \]

\[ i = v_1 W_1(\varphi_1, \varphi_2) = v_2 W_2(\varphi_2, \varphi_1) \]

\[ \varphi_{12} = \varphi_1 + \varphi_2 \]

\[ i = v_1(\alpha_1 \varphi_1 + \beta_1 + \kappa_2 \varphi_2) = v_2(\alpha_2 \varphi_2 + \beta_2 + \kappa_1 \varphi_1) \]
Coupled MRs in Serial Connections

**Serial MR Circuit with Identical Polarities**

\[
\frac{d\phi_1}{dt} = \frac{v_{12}(\alpha_2\phi_2 + \beta_2 + \kappa_1\phi_1)}{(\alpha_1 + \kappa_1)\phi_1 + (\alpha_2 + \kappa_2)\phi_2 + \beta_1 + \beta_2}
\]

\[
\frac{d\phi_2}{dt} = \frac{v_{12}(\alpha_1\phi_1 + \beta_1 + \kappa_2\phi_2)}{(\alpha_1 + \kappa_1)\phi_1 + (\alpha_2 + \kappa_2)\phi_2 + \beta_1 + \beta_2}
\]
Coupled MRs in Serial Connections

For the special case of $\alpha_1 = \alpha_2 = \alpha$ and $\kappa_1 = \kappa_2 = \alpha$, 

$$\frac{d\phi_1}{dt} = \frac{\alpha \phi_{12} + \beta_2}{2\alpha \phi_{12} + \beta_1 + \beta_2} \nu_{12}$$

$$\frac{d\phi_2}{dt} = \frac{\alpha \phi_{12} + \beta_1}{2\alpha \phi_{12} + \beta_1 + \beta_2} \nu_{12}$$
Coupled MRs in Serial Connections

Assume that the initial value of $\varphi_{12}$ is zero,

$$\varphi_1 = \frac{1}{4\alpha} \left[ 2\alpha \varphi_{12} + (\beta_2 - \beta_1) \ln(2\alpha \varphi_{12} + \beta_1 + \beta_2) \right]$$

$$\varphi_2 = \frac{1}{4\alpha} \left[ 2\alpha \varphi_{12} + (\beta_1 - \beta_2) \ln(2\alpha \varphi_{12} + \beta_1 + \beta_2) \right]$$

Memductance of individual MR can be obtained,

$$W_1(\varphi_1, \varphi_2) = \alpha_1 \varphi_1 + \beta_1 + \kappa_2 \varphi_2$$

$$W_2(\varphi_2, \varphi_1) = \alpha_2 \varphi_2 + \beta_2 + \kappa_1 \varphi_1$$
Coupled MRs in Serial Connections

For further simplification we assume $\beta_1=\beta_2=\beta$,

$$\varphi_1 = \varphi_2 = \frac{1}{2} \varphi_{12}$$

$$\nu_1 = \nu_2 = \frac{1}{2} \nu_{12}$$

The memductance of each coupled MR can be written as,

$$W_1 = W_2 = \alpha \varphi_{12} + \beta$$

Two coupled MRs serially connected with identical polarities operate as a new MR with a new memductance value of $W_{12}=W_1/2=W_2/2=(\alpha \varphi_{12}(t)+\beta)/2$. 
Coupled MRs in Serial Connections - Simulation Results

**Serial MR Circuit with Identical Polarities**

\[ W_{12} = \frac{W_1 W_2}{W_1 + W_2} \]

Identical Polarities

![Graph showing memductance and voltages](image)

Initial Memductance

![Graph showing memductance with initial flux](image)
Coupled MRs in Parallel Connections

**Parallel MR Circuit with Identical Polarities**

\[ i = i_1 + i_2 \]

\[ \phi_{12} = \phi_1 = \phi_2 \]

\[ i = v_1 (\alpha_1 \phi_1 + \beta_1 + \kappa_2 \phi_2) + v_2 (\alpha_2 \phi_2 + \beta_2 + \kappa_1 \phi_1) \]

\[ q = \frac{1}{2} (\alpha_1 + \alpha_2 + \kappa_1 + \kappa_2) \phi_{12}^2 + (\beta_1 + \beta_2) \phi_{12} \]
Coupled MRs in Parallel Connections

Parallel MR Circuit with Identical Polarities

\[ W_{12}(\phi_{12}) = \frac{dq(\phi_{12})}{d\phi_{12}} = (\alpha_1 + \alpha_2 + \kappa_1 + \kappa_2)\phi_{12} + \beta_1 + \beta_2 \]

Two flux coupled MRs in parallel connection operates as a new flux controlled MR, and the equivalent memductance is equal to the sum of individual memductances.
Coupled MRs in Parallel Connections - Simulation Results

**Parallel MR Circuit with Identical Polarities**

![Diagram of parallel MR circuit with identical polarities](image)

- **A1** and **B2** represent the terminals of the MRs.
- **MR1** and **MR2** are the magnetic reluctance devices.
- **v12** is the voltage across the parallel connection.
- **i1**, **i2**, **i12** are the currents in the circuit.
- **W1**, **W2**, **W12** are the memductance coefficients.

**Graphs**

- Left graph: Relationships between **v12** and currents **i1**, **i2**, **i12**.
- Right graph: Memductance **W12** vs. **φ12** (Wb).

**Identical Polarities**

- Lines with different **α2** values indicating the memductance characteristics for parallel MR connections.

---

*Note: The graphs and diagram are used to illustrate the simulation results for the parallel MR circuit with identical polarities.*
Conclusion

- A memristor based chaotic circuit is constructed.
- A universal mutator for transformations of memristor, memcapacitor and meminductor is developed.
- Dynamic behaviour of coupled memristor based circuits is studied.
Future work

- Study other circuit elements with memory: memcapacitor and meminductor.
- Develop other applications of memristor based circuits, e.g. synchronization and consensus of coupled memristor based circuits.
References